PATENT ABSTRACTS OF JAPAN

(11)Publication number : 04-140716
(43)Date of publication of application : 14.05.1992

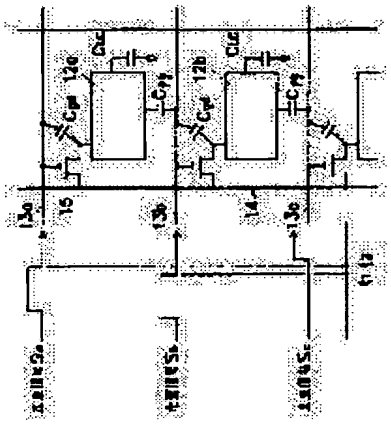
(51)Int.Cl. G02F 1/133
G09G 3/36

(21)Application number : 02-264578
(22)Date of filing : 01.10.1990

(71)Applicant : SHARP CORP
(72)Inventor : MATSUMOTO TOSHIO
TANAKA MASASHI
KATO KENICHI

(54) LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:
PURPOSE: To equalize potentials held by respective picture element electrodes and to form an uniform display image by connecting the picture element electrode to a data signal line through a switching element which is controlled through a scanning signal line.
CONSTITUTION: When scanning signals Sa and Sb are applied to scanning signal lines 13a and 13b at the same time, the application of the signal Sb between picture element electrodes 12a and 12b is completed earlier. At this time, there is no variation in potential on a signal line 13c. The potential of the electrode 12a which is adjacent across a floating capacitor Cpg drops under the influence, but the electrode 12a is connected to a data signal line 14, so the potential recovers to the potential of data signal by charging. Then when the application of the signal Sa to the signal line 13a ends later, the variation in the potential of the adjacent signal line 13b already ends, so the same condition with the case of the electrode 12b is obtained and the drop potential has the same value. Consequently, the potentials that the respective picture element electrodes hold become equal and the uniform display image can be obtained.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

(19)日本国特許庁（ＪＰ）　(12)特　許　公　報（Ｂ２）　(11)特許番号

第2625248号

(45)発行日　平成９年(1997)７月２日　(24)登録日　平成９年(1997)４月11日

(51)Int.Cl.[6]		識別記号	庁内整理番号	Ｆ Ｉ		技術表示箇所
Ｇ０２Ｆ	1/133	５５０		Ｇ０２Ｆ	1/133	５５０
		５２５				５２５
Ｇ０９Ｇ	3/36			Ｇ０９Ｇ	3/36	

請求項の数１(全 10 頁)

(21)出願番号　特願平2－264578

(22)出願日　平成２年(1990)10月１日

(65)公開番号　特開平4－140716

(43)公開日　平成４年(1992)５月14日

(73)特許権者　999999999
シャープ株式会社
大阪府大阪市阿倍野区長池町22番22号

(72)発明者　松本　俊夫
大阪府大阪市阿倍野区長池町22番22号
シャープ株式会社内

(72)発明者　田中　匡祉
大阪府大阪市阿倍野区長池町22番22号
シャープ株式会社内

(72)発明者　加藤　憲一
大阪府大阪市阿倍野区長池町22番22号
シャープ株式会社内

(74)代理人　弁理士　山本　秀策

審査官　小橋　立昌

(54)【発明の名称】　液晶表示装置

1

(57)【特許請求の範囲】

【請求項１】走査信号線によってスイッチングが制御されるスイッチング素子を介して画素電極がデータ信号線に接続された液晶パネルを備え、隣接する複数本の走査信号線に同時に走査信号を印加する走査信号線駆動回路が設けられたアクティブマトリクス方式の液晶表示装置であって、

走査信号が同時に印加される隣接した２本の走査信号線について、これらの走査信号線にそれぞれスイッチング素子を介して接続された２列の画素電極の間に位置する走査信号線の側に印加した走査信号を他方の走査信号線に印加した走査信号よりも早いタイミングで印加を終了させる走査信号タイミング制御回路を備えている液晶表示装置。

【発明の詳細な説明】

2

(産業上の利用分野)

本発明は、カラーテレビジョン画像の表示等に用いられるアクティブマトリクス方式の液晶表示装置に関する。

(従来の技術)

NTSC等のカラーテレビジョン方式では、１画面（フレーム）の走査を奇数フィールドと偶数フィールドとに分け、それぞれのフィールドにおいて走査線を１本ずつ飛び越して走査を行うインターレース方式が採用されている。そして、液晶表示装置において、このような映像信号をインターレース方式に準拠した高解像度で表示しようとする場合、２本同時走査方式が用いられる。

ここで、液晶表示装置におけるTFTアクティブマトリクス基板の構成を第７図に示す。このTFTアクティブマトリクス基板は、基板11上に多数の走査信号線13とデー

タ信号線14とを形成すると共に、これらにTFT（薄膜トランジスタ）15を介して画素電極12をそれぞれマトリクス状に接続したものである。また、このTFTアクティブマトリクス基板の対向面には、図示しない共通の対向電極が液晶層を介して配置されている。この構成により、各走査信号線13に走査信号が印加されると、導通したTFT15を介して当該走査信号線13に接続された画素電極12に各データ信号線14のデータ信号が送り込まれることになる。そして、走査信号の印加が終了しTFT15が遮断した後も、各画素電極12には、液晶層の容量等によってデータ信号の電位が保持され、この電位が走査信号の印加の度に更新されるようになる。従って、走査信号線に走査信号を順に印加するマトリクス方式であっても、各画素電極12では、常時データ信号の電位を保持し液晶層に印加することができる。

上記２本同時走査方式は、このような液晶表示装置において、隣接する２本の走査信号線13に同時に走査信号を印加するようにしたものである。即ち、例えば第８図に示すように、奇数フィールドの走査においては、まず１本目と２本目の走査信号線13に同時に走査信号を印加し、次に１水平走査期間遅れて３本目と４本目の走査信号線13に同時に走査信号を印加するというように、奇数本目の走査信号線13とこの次に位置する偶数本目の走査信号線13に同時に走査信号を順次印加するようにし、偶数フィールドの走査においては、まず１本目の走査信号線13に走査信号を印加し、次に１水平走査期間遅れて２本目と３本目の走査信号線13に同時に走査信号を印加し、さらに４本目と５本目の走査信号線13というように、奇数フィールドの走査時とは組み合わせの異なる隣接した２本の走査信号線13に同時に走査信号を印加するようにしている。従って、これまでの走査信号線13に１本ずつ走査信号を印加する単純走査方式の場合に比べ、約倍の走査信号線13や画素電極12が必要になるが、インターレース方式に準拠した高解像度の画像を得ることができるようになる。

（発明が解決しようとする課題）

ところで、上記の走査信号線13に走査信号を印加した場合、これに接続された画素電極12の電位は、走査信号の印加終了時にTFT15におけるゲート－ドレイン間の寄生容量Cgdの影響を受けてデータ信号の電位よりも低下することになる。即ち、単純走査方式の場合には、TFT15における導通時と遮断時のゲート電圧をそれぞれVGH、VGLとし、画素電極12における液晶層の容量をCLCとすると、おおよそ次式（１）で示される電位ΔVだけデータ信号の電位よりも低下することになる。

$$\Delta V = (VGH - VGL) \times Cgd / (CLC + Cgd) \quad \cdots (1)$$

もっとも、単純走査方式の場合には、このような電位低下は全画素電極12について共通である。このため、対向電極に印加する対向電圧を低下電位ΔVだけシフトすれば、交流駆動によって液晶層に印加される電圧のDCバランスを０に維持することは容易である。

しかしながら、上記２本同時走査方式の場合には、第９図に示すように、寄生容量Cgdの他に、画素電極12とこの画素電極12には接続されない側に隣接する走査信号線13との間の浮遊容量Cpgの影響も考慮しなければならない。即ち、図示の走査信号線13a、13bに走査信号Sa、Sbを印加した場合、これらの走査信号線13a、13b間に位置する画素電極12aについては、接続されない側に隣接する走査信号線13bも走査信号Sbによって電位の変化が生じるため、走査信号Saの印加終了時における低下電位ΔVは次式（２）で示されるものとなる。

$$\Delta V1 = (VGH - VGL) \times (Cgd + Cpg) / (CLC + Cgd + Cpg) \quad \cdots (2)$$

ところが、他方の画素電極12bについては、接続されない側に隣接する走査信号線13cにはまだ走査信号が印加されていないために電位の変化がないので、低下電位ΔVは次式（３）で示されるようになる。

$$\Delta V2 = (VGH - VGL) \times Cgd / (CLC + Cgd + Cpg) \quad \cdots (3)$$

このため、画素電極12aと画素電極12bとは、同じデータ信号線14に接続され同じデータ信号電圧が与えられているにもかかわらず、走査信号の印加終了時の低下電位にΔV1とΔV2との差が生じ、その後の保持電位は画素電極12bの方が高電位となる。

従って、従来の液晶表示装置では、同時に複数の走査信号線に走査信号を印加した場合、同じデータ信号線上で隣接する画素の明るさに差が生じ、画像品質が低下するという問題が生じていた。

本発明は、上記事情に鑑み、２本の走査信号線における走査信号の印加終了時期をずらして、それぞれの画素電極が同じ条件で電位を保持できるようにすることにより、同時に複数の走査信号線に走査信号を印加する駆動方式においても画素の明るさにムラの生じることのない液晶表示装置を提供することを目的としている。

（課題を解決するための手段）

本発明の液晶表示装置は、走査信号線によってスイッチングが制御されるスイッチング素子を介して画素電極がデータ信号線に接続された液晶パネルを備え、隣接する複数本の走査信号線に同時に走査信号を印加する走査信号線駆動回路が設けられたアクティブマトリクス方式の液晶表示装置であって、走査信号が同時に印加される隣接した２本の走査信号線について、これらの走査信号線にそれぞれスイッチング素子を介して接続された２列の画素電極の間に位置する走査信号線の側に印加した走査信号を他方の走査信号線に印加した走査信号よりも早いタイミングで印加を終了させる走査信号タイミング制御回路を備えており、そのことにより上記目的が達成される。

（作用）

上記構成により、第１図に示す走査信号線13a、13bに

5

同時に走査信号Sa、Sbを印加した場合、まずこれらの走査信号線13a、13bに接続された画素電極12a、12b間に位置する走査信号線13bの走査信号Sbが時刻t1において先に印加を終了する。そして、この際の画素電極12bにおける低下電位ΔVは、従来の場合と同様に走査信号線13cに電位の変化がないため、上記式（3）と同じ次式で示されるものとなる。

$$\Delta V = (VGH - VGL) \times Cgd / (CLC + Cgd + Cpg) \quad \cdots (4)$$

また、このように走査信号線13bの走査信号Sbが先に印加を終了すると、浮遊容量Cpgを介して隣接する画素電極12aの電位も影響を受けて一旦低下する。しかし、この場合には、まだTFT15が導通状態であり画素電極12aがデータ信号線14に接続されているため、直ちに充電が行われ再びデータ信号の電位に復帰する。そして、この後の時刻t2に走査信号線13aの走査信号Saが遅れて印加を終了すると、既に隣接する走査信号線13bの電位が変化を終了しているために画素電極12bの場合と同じ条件となり、低下電位ΔVも上記式（4）と同じ値となる。

この結果、本発明の液晶表示装置によれば、２本の走査信号線に同時に走査信号を印加した場合にも、この走査信号の印加終了時における電位低下が同じものとなるので、各画素電極が保持する電位が等しくなり均一な表示画像を得ることができるようになる。

なお、各走査信号線への走査信号の印加時間を均一にするために、走査信号の印加開始のタイミングも、この終了のタイミングに合わせてシフトするようにしてもよい。また、３本以上の走査信号線に同時に走査信号を印加するような場合にも、隣接する２本ずつの走査信号線間で順に走査信号の印加終了のタイミングをずらすことにより、同様に実施可能である。

（実施例）

本発明を実施例について以下に説明する。

第２図乃至第６図は本発明の一実施例を示すものであって、第２図は液晶表示装置のブロック図、第３図は走査信号線駆動回路のブロック図、第４図は走査信号線駆動回路の動作を示すタイムチャート、第５図は液晶表示装置における奇数フィールド走査時の動作を示すタイムチャート、第６図は液晶表示装置における偶数フィールド走査時の動作を示すタイムチャートである。なお、第７図乃至第９図に示した従来例と同様の機能を有する構成要素には同じ符号を付する。

本実施例は、NTSC方式のカラーテレビジョンの画像を液晶パネルに表示するための液晶表示装置である。

液晶表示装置における液晶パネル１のTFTアクティブマトリクス基板は、前記第７図に示すように、基板上に多数の画素電極12と走査信号線13とデータ信号線14とTFT15とを形成したものである。そして、各画素電極12は、第１図に示すように、TFT15のソースードレイン端子間を介して隣接するデータ信号線14に接続されている。また、この各TFT15は、ゲート端子が隣接する走査信号線13に接続され、この走査信号線13に高レベル電圧の走査信号が印加されると、ソースードレイン端子間を導通するようになっている。

6

上記液晶パネル１のTFTアクティブマトリクス基板は、第２図に示すように、各走査信号線13が１本おきの偶数本目と奇数本目とを左右に振り分けて引き出されている。そして、この奇数本目の各走査信号線13は、走査信号線駆動回路２に接続され、偶数本目の各走査信号線13は、走査信号線駆動回路３に接続されている。これらの走査信号線駆動回路２、３は、第３図に示すように、クロック信号に従ってスタート信号を順次シフトさせるシフトレジスタ回路2a、3aと、このシフトレジスタ回路2a、3aの出力をTFT15の駆動に必要なレベルに引き上げるレベルシフタ回路2b、3bと、このレベルシフタ回路2b、3bの出力を保持し各走査信号線13に出力する出力バッファ2c、3cからなる。また、この走査信号線駆動回路２、３のシフトレジスタ回路2a、3aには、第２図に示すように、タイミング制御回路４からそれぞれ走査信号の基礎となるスタート信号と水平走査期間周期のクロック信号が入力されるようになっている。従って、これらの走査信号線駆動回路２、３に接続された各走査信号線13には、第４図に示すように、スタート信号を順次シフトさせた走査信号が水平走査期間ずつ遅れて出力されることになる。なお、この場合、各走査信号は、先のクロック信号の立ち下がりに同期して印加が開始され、後のクロック信号の立ち上がりに同期して印加が終了する。

上記タイミング制御回路４は、映像信号から分離した同期信号に基づいてスタート信号とクロック信号とを出力するようになっている。即ち、スタート信号については、垂直同期信号に同期して、奇数フィールドの走査時には走査信号線駆動回路２、３に同時に出力し、偶数フィールドの走査時には走査信号線駆動回路３へのスタート信号を走査信号線駆動回路２よりも１水平走査期間だけ遅らせて出力する。また、クロック信号は、奇数フィールドの走査時に走査信号線駆動回路２よりも走査信号線駆動回路３側の位相を僅かに進ませ、偶数フィールドの走査時に走査信号線駆動回路２よりも走査信号線駆動回路３側の位相を僅かに遅らせて出力するようになっている。

上記構成の液晶表示装置の動作を第５図及び第６図に基づいて説明する。

インターレース方式により奇数フィールドの走査が行われる場合には、タイミング制御回路４からのスタート信号が走査信号線駆動回路２、３に同時に出力されるので、まず１本目と２本目の走査信号線13に同時に走査信号が印加され、次に水平走査期間だけ遅れて３本目と４本目の走査信号線13に同時に走査信号が印加され、以降同様に奇数本目とこれに続く偶数本目との２本の走査信号線13に順次走査信号が印加されることになる。また、

偶数フィールドの走査が行われる場合には、タイミング制御回路４から走査信号線駆動回路２に先にスタート信号が出力され、走査信号線駆動回路３には１水平走査期間だけ遅れてスタート信号が出力される。このため、まず１本目の走査信号線13に走査信号が印加されると、次に水平走査期間だけ遅れて２本目と３本目の走査信号線13に同時に走査信号が印加され、以降偶数本目とこれに続く奇数本目との２本の走査信号線13に順次走査信号が印加されることになる。この結果、液晶パネル１の各画素は、奇数フィールドで奇数本目とこれに続く偶数本目の走査線の表示が行われ、偶数フィールドでは偶数本目とこれに続く奇数本目の走査線の表示が行われることになり、これによってインターレース方式に準じた２本同時走査方式による高解像度の画像を表示することができるようになる。

また、上記奇数フィールドにおいては、タイミング制御回路４が走査信号線駆動回路３へのクロック信号の位相を僅かに進めるために、同時に印加される走査信号は、実際には、奇数本目の走査信号線13よりも偶数本目の走査信号線13の方が僅かに早く印加を開始し、印加終了時期も早くなる。従って、この奇数フィールドの走査においては、第１図に示した走査信号線13aが奇数本目の走査信号線13に対応し、走査信号線13bが偶数本目の走査信号線13対応することになる。このため、先に走査信号の印加が終了する偶数本目の走査信号線13（13b）に接続された画素電極12（12b）に保持される電位は、隣接する接続されない走査信号線13（13c）の電位が変化しないことから、データ信号の電位より前記式（４）で示した低下電位ΔＶだけ低い値となる。そして、これより遅れて走査信号の印加が終了する奇数本目の走査信号線13（13a）に接続された画素電極12（12a）に保持される電位も、隣接する接続されない先の走査信号線13（13b）が既に電位を変化し終えているため、上記と同じ低下電位ΔＶだけ低い値となる。

さらに、上記偶数フィールドにおいては、タイミング制御回路４が走査信号線駆動回路３へのクロック信号の位相を僅かに遅らせるために、同時に印加される走査信号は、実際には、偶数本目の走査信号線13よりも奇数本目の走査信号線13の方が僅かに早く印加を開始し、印加終了時期も早くなる。従って、この偶数フィールドの走査においては、第１図に示した走査信号線13aが偶数本目の走査信号線13に対応し、走査信号線13bが奇数本目の走査信号線13に対応することになる。このため、先に走査信号の印加が終了する奇数本目の走査信号線13（13b）に接続された画素電極12（12b）に保持される電位は、隣接する接続されない走査信号線13（13c）の電位が変化しないことから、データ信号の電位より上記と同じ低下電位ΔＶだけ低い値となる。そして、これより遅れて走査信号の印加が終了する偶数本目の走査信号線13（13a）に接続された画素電極12（12a）に保持される電位も、隣接する接続されない先の走査信号線13（13b）が既に電位を変化し終えているため、上記と同じ低下電位ΔＶだけ低い値となる。

以上の結果、本実施例の液晶表示装置によれば、インターレース方式に準じた２本同時走査方式によって２本の走査信号線13に同時に走査信号を印加した場合にも、この走査信号の印加終了時における条件が各走査線ごとに同一となり、各画素電極12が保持する電位が等しくなるので、均一な表示画面を得ることができる。

（発明の効果）

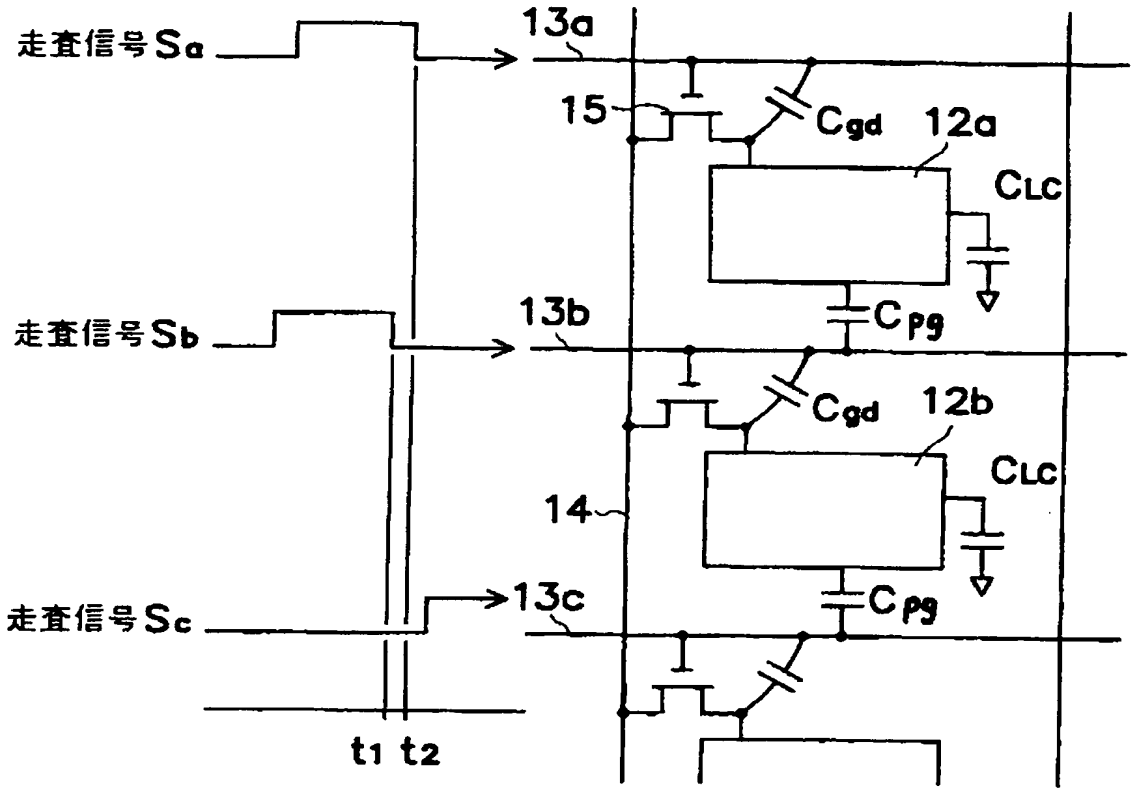
以上の説明から明らかなように、本発明の液晶表示装置によれば、隣接する複数の走査信号線に同時に走査信号を印加した場合にも、これらの走査信号の印加終了時における電位低下を同じものとすることができるので、各画素電極が保持する電位が等しくなり均一な表示画像を得ることができるようになる。

【図面の簡単な説明】

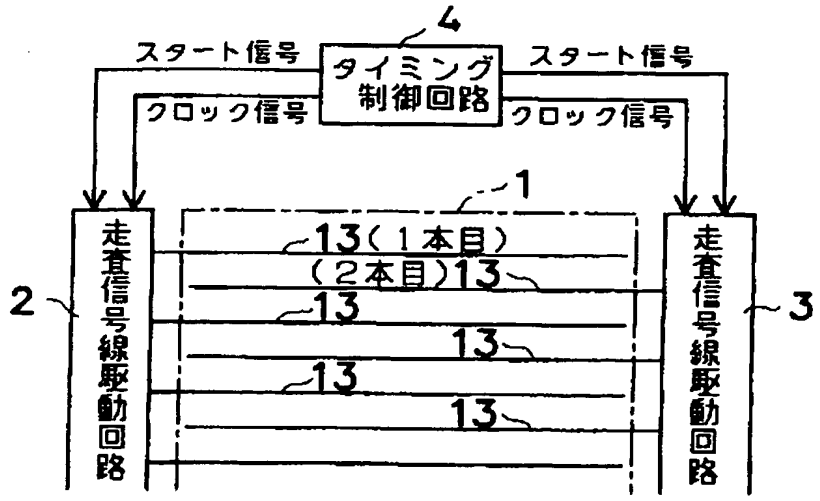
第１図は本発明の作用を説明するためのアクティブマトリクス基板上の回路図、第２図乃至第６図は本発明の一実施例を示すものであって、第２図は液晶表示装置のブロック図、第３図は走査信号線駆動回路のブロック図、第４図は走査信号線駆動回路の動作を示すタイムチャート、第５図は液晶表示装置における奇数フィールド走査時の動作を示すタイムチャート、第６図は液晶表示装置における偶数フィールド走査時の動作を示すタイムチャート、第７図乃至第９図は従来例を示すものであって、第７図はTFTアクティブマトリクス基板の部分拡大平面図、第８図は２本同時走査方式の動作を説明するためのタイムチャート、第９図はアクティブマトリクス基板上の回路図である。

１……液晶パネル、２、３……走査信号線駆動回路、４……タイミング制御回路、12……画素電極、13……走査信号線、14……データ信号線、15……TFT（スイッチング素子）。

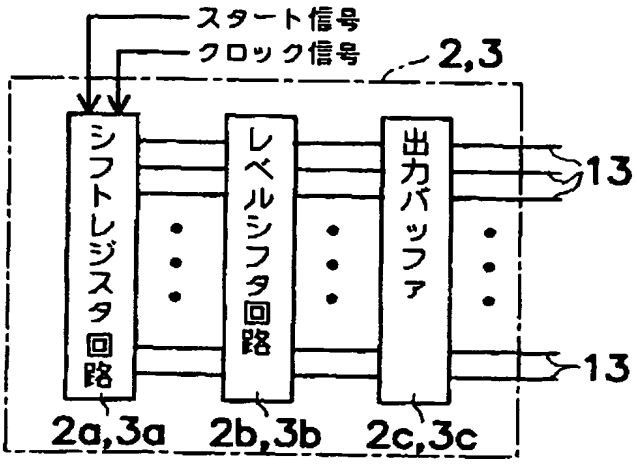
【第1図】


走査信号Sa
走査信号Sb
走査信号Sc
13a
13b
13c
15
14
Cgd
12a
12b
CLC
Cpg
t1 t2

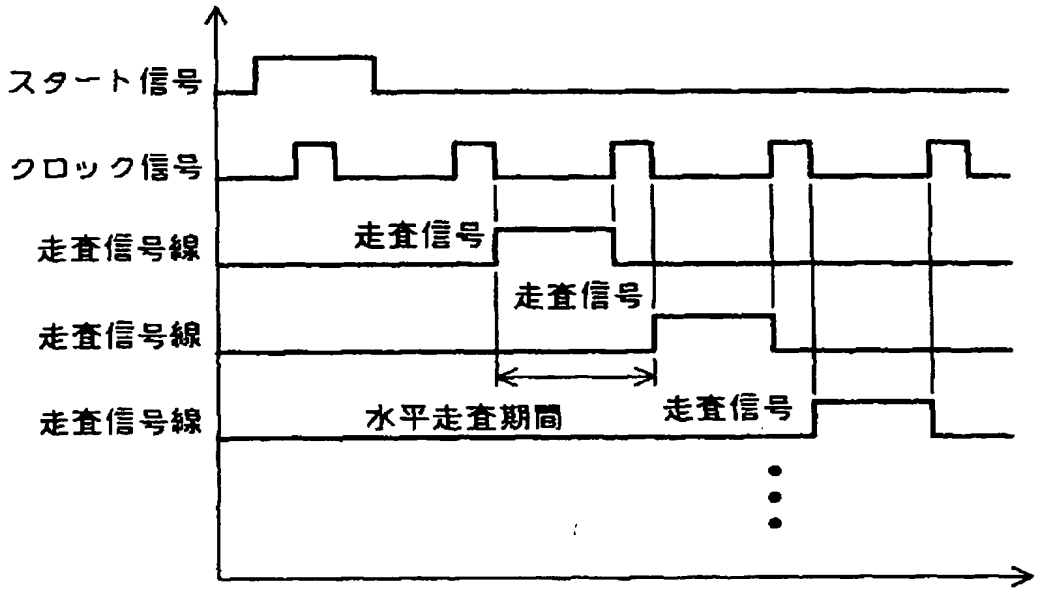
【第2図】


4
スタート信号
タイミング制御回路
スタート信号
クロック信号
クロック信号
1
走査信号線駆動回路
2
13(1本目)
(2本目)13
13
13
13
13
走査信号線駆動回路
3

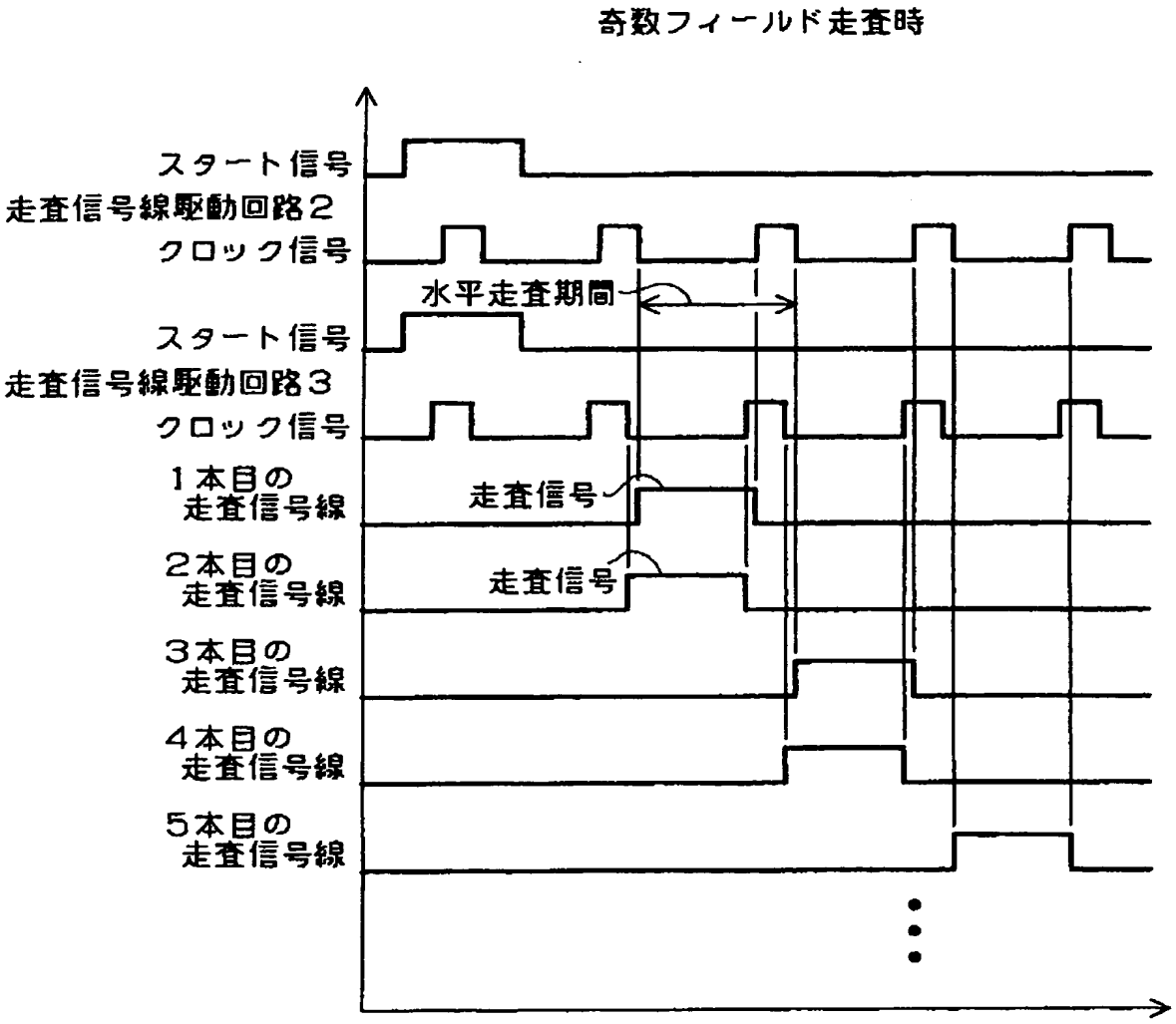
【第3図】


スタート信号
クロック信号
2,3
シフトレジスタ回路
レベルシフタ回路
出力バッファ
13
13
2a,3a
2b,3b
2c,3c

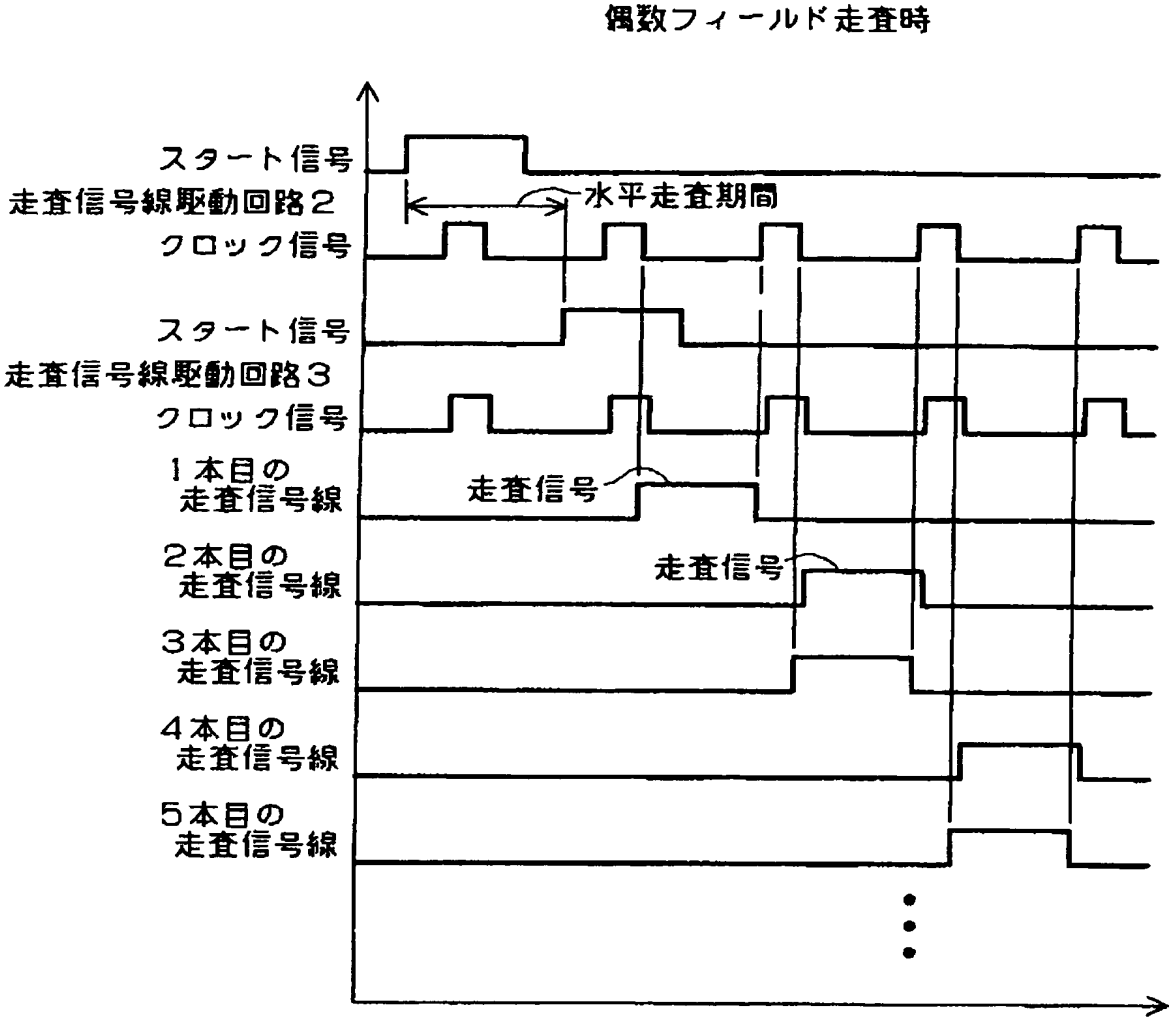
【第4図】


スタート信号
クロック信号
走査信号線
走査信号
走査信号線
走査信号
走査信号線
水平走査期間
走査信号

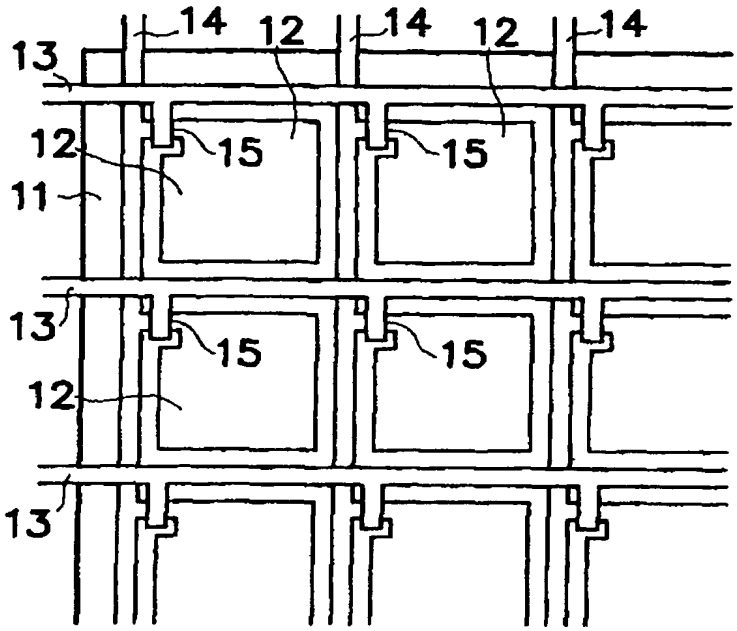
【第5図】


奇数フィールド走査時
スタート信号
走査信号線駆動回路2
クロック信号
水平走査期間
スタート信号
走査信号線駆動回路3
クロック信号
1本目の
走査信号線
走査信号
2本目の
走査信号線
走査信号
3本目の
走査信号線
4本目の
走査信号線
5本目の
走査信号線

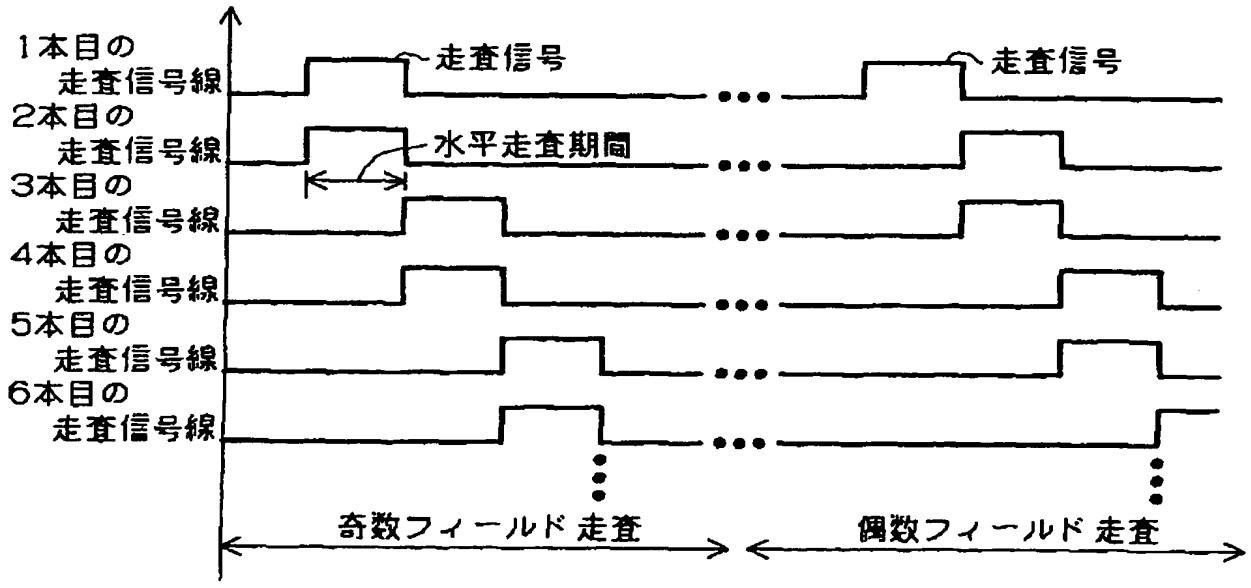
【第6図】


偶数フィールド走査時
スタート信号
走査信号線駆動回路２
水平走査期間
クロック信号
スタート信号
走査信号線駆動回路３
クロック信号
１本目の
走査信号線
走査信号
２本目の
走査信号線
走査信号
３本目の
走査信号線
４本目の
走査信号線
５本目の
走査信号線

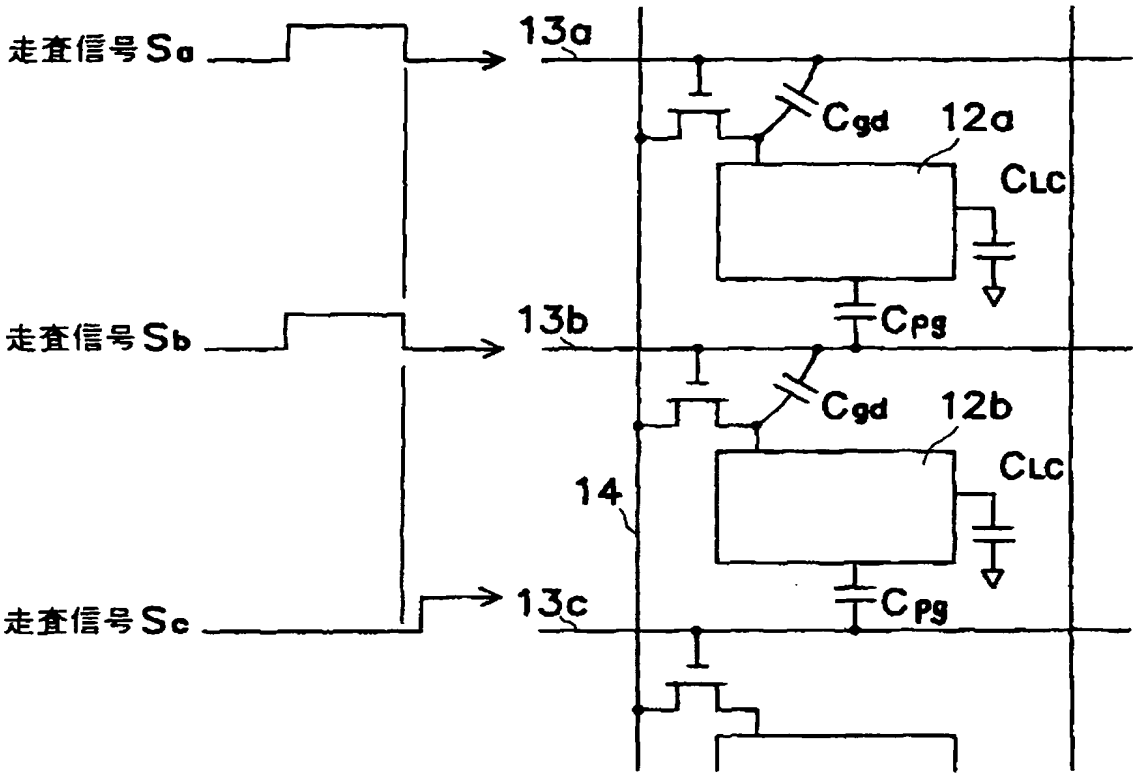
【第7図】


14
12
14
12
14
13
12
15
15
11
13
15
15
12
13

【第8図】


1本目の
走査信号線
2本目の
走査信号線
3本目の
走査信号線
4本目の
走査信号線
5本目の
走査信号線
6本目の
走査信号線
走査信号
走査信号
水平走査期間
奇数フィールド走査
偶数フィールド走査

【第9図】


走査信号Sa
走査信号Sb
走査信号Sc
13a
13b
13c
14
Cgd
12a
CLC
Cpg
Cgd
12b
CLC
Cpg

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An output control circuit, which is used together with ~~transfer means~~a transfer device in which a ~~number~~ plurality of unit circuits that shift a starting pulse sequentially in synchronization with a clock signal are in cascade connection with each other, and ~~generates~~generate a set of a positive logic output signal and a negative logic output ~~signal which~~signal, which is an inversion of the positive logic output ~~signal based~~signal, based on an output signal from each of the unit circuits, the output control circuit ~~having,~~comprising:

a first logic operation unit which, based on an output signal from a unit circuit and an output signal from a subsequent-stage unit circuit, generates an output signal that is enabled in a period while the output signals from the two unit circuits are enabled at the same ~~time, and,~~time; and

a second logic operation unit which generates the positive logic output signal and the negative logic output signal based on the output signal from the first logic operation unit, and controls an enabling period of at least one of the positive logic output signal ~~or~~ and the negative logic output signal based on the output signal from a first logic operation unit in a subsequent-stage output control circuit.

2. (Currently Amended) The output control circuit according to claim 1, ~~characterized in that~~

the second logic operation unit ~~has~~ having a first system that generates the positive logic output signal based on the output signal from the first logic operation unit, and a second system that generates the negative logic output signal based on the output signal from the first logic operation unit,

~~wherein~~ one of a system, the first system or the second system, having a longer delay time, ~~has~~ having a logic circuit that controls an enabling period of the positive logic output signal or the negative logic output signal which should be generated in one of the system based on the output signal from the first logic operation unit in the subsequent-stage output control circuit.

3. (Currently Amended) The output control circuit according to claim 2, ~~characterized in that~~

the output signal from the first logic operation unit ~~is~~ being enabled at low level, and

~~and~~ the logic circuit in the second logic operation unit ~~is~~ being a NAND circuit that is included in the second system, and controls the enabling period of the negative logic output signal based on the output signal from the first logic operation unit in the subsequent-stage output control circuit.

4. (Currently Amended) The output control circuit according to claim 3, ~~characterized in that~~

the output signal from the unit circuit ~~is~~ being enabled at high level,

the first logic operation unit ~~has~~ having a NAND circuit,

the first system in the second logic operation unit ~~has~~ having a first inverting circuit that inverts an output signal from the NAND circuit in the first logic operation unit and then outputs the signal as the positive logic output signal,

the second system in the second logic operation unit ~~has~~ having a second inverting circuit that inverts the output signal from the NAND circuit in the first logic operation unit and then outputs the signal, and the logic circuit that operates inversion of a logical product of the output signal from the second inverting circuit and the output signal

from the first logic operation unit in the subsequent-stage output control circuit and then outputs the inversion of the logical product as the negative logic output signal.

5. (Currently Amended) The output control circuit according to claim 2, ~~characterized in that~~

the output signal from the first logic operation unit ~~is~~ being enabled at high level, and

~~and~~ the logic circuit in the second logic operation unit ~~is~~ being a NOR circuit that is included in the first system, and controls the enabling period of the positive logic output signal based on the output signal from the first logic operation unit in the subsequent-stage output control circuit.

6. (Currently Amended) The output control circuit according to claim 5, ~~characterized in that~~

the output signal from the unit circuit ~~is~~ being enabled at low level,

the first logic operation unit ~~has~~ having a NOR circuit,

the second system in the second logic operation unit ~~has~~ having a first inverting circuit that inverts an output signal from the NOR circuit in the first logic operation unit and then outputs the signal as the negative logic output signal, and

the first system in the second logic operation unit ~~has~~ having a second inverting circuit that inverts the output signal from the NOR circuit in the first logic operation unit and then outputs the signal, and the logic circuit that operates the inversion of the logical sum of the output signal form the second inverting circuit and the output signal from the first logic operation unit in the subsequent-stage output control circuit and then outputs the inversion of the logical sum as the positive logic output signal.

7. (Currently Amended) The output control circuit according to claim 2, further comprising ~~characterized by having~~ a level conversion circuit that converts amplitude of signal in a previous stage of the logic circuit.

8. (Currently Amended) The output control circuit according to claim 7, ~~characterized in that~~

the output signal from the unit circuit ~~is~~ being enabled at high level,

the first logic operation unit ~~has~~ having the NAND circuit, and

the second logic operation unit ~~has~~ having the second inverting circuit that inverts the output signal from the NAND circuit in the first logic operation unit,

the level conversion circuit that converts an amplitude of each signal of the output signal from the NAND circuit in the first logic operation unit and the output signal from the second inverting circuit and then outputs the signal,

a first inverting circuit that inverts the output signal, which is level converted, from the NAND circuit in the first logic operation unit, and then outputs the signal as the positive logic output signal, and

the logic circuit that operates the inversion of the logical product of the output signal, which is level converted, from the second inversion circuit, and the output signal, which is level converted in the subsequent-stage output control circuit, from the first logic operation unit, and then outputs the inversion of the logical product as the negative logic output signal.

9. (Currently Amended) The output control circuit according to claim 7, ~~characterized in that~~

the output signal from the unit circuit ~~is~~ being enabled at low level,

the first logic operation unit ~~has~~ having the NOR circuit, and

the second logic operation unit ~~has~~ having a second inverting circuit that inverts the output signal from the NOR circuit in the first logic operation unit,

the level conversion circuit that converts the amplitude of each signal of the output signal from the NOR circuit in the first logic operation unit and the output signal form the second inverting circuit and then outputs the signal,

a first inverting circuit that inverts the output signal, which is level converted, from the NOR circuit in the first logic operation unit, and then outputs the signal as the negative logic output signal, and

the logic circuit that operates the inversion of the logical sum of the output signal, which is level converted, from the second inverting circuit, and the output signal, which is level converted in the subsequent-stage output control circuit, from the first logic operation unit, and then outputs the inversion of the logical sum as the positive logic output signal.

10. (Currently Amended) The output control circuit according to claim 1, further comprising ~~characterized by having~~ an electric current amplification unit that is provided in a later stage of the second logic operation unit and performs an electric current amplification for respective output signals from the second logic operation unit and then outputs the signals as the positive logic output signal and the negative logic output signal.

11. (Currently Amended) The output control circuit according to claim 1, further including ~~characterized by having~~ a holding unit, provided in a later stage of the second logic operation unit, that holds ~~for holding~~ respective output signals from the second logic operation unit bi-directionally, ~~wherein~~ respective signals from the holding unit ~~are~~ being output as the positive logic output signal and the negative logic output signal.

12. (Currently Amended) A driving circuit, which drives an electro-optic apparatus having a number of scan lines, a number of data lines, pixel electrodes and

switching elements arranged in a matrix pattern corresponding to intersections of the scan lines and the data lines, the driving circuit ~~characterized by having,~~comprising:

a transfer ~~means~~ device in which unit circuits that shifts a starting pulse sequentially in synchronization with a clock signal are in a cascade connection with each other, and

an output control ~~means~~ device having a number of the output control circuits according to claim 1.

13. (Currently Amended) An electro-optic apparatus, ~~characterized by having,~~comprising:

a number of the scan ~~lines,~~lines;

a number of the data ~~lines,~~lines;

the pixel electrodes and the switching elements arranged in a matrix pattern corresponding to the intersections of the scan lines and the data lines,

a image signal line through which an image signal is supplied,

a number of switching circuits provided corresponding to each of the data lines, in which an on/off control is performed by a set of a control signal that is enabled at high level and a control signal that is enabled at low level, and one terminal is connected to the data line and the other terminal is connected to the image signal line, and

the driving circuit according to claim 12, which supplies the positive logic output signal and the negative logic output signal to each of the switching circuits as the set of the control signals.

14. (Currently Amended) An electronic instrument, comprising ~~characterized by having~~ the electro-optic apparatus according to claim 13.

REMARKS

Claims 1-14 are pending in this application. By this Preliminary Amendment, the specification, Abstract, and claims 1-14 are amended. No new matter is added.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

John S. Kern
Registration No. 42,719

JAO:JSK/kap

Attachments:
Amended Abstract
Substitute Specification
Marked-up copy of specification

Date: October 20, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

ABSTRACT OF THE DISCLOSURE

~~A~~ The invention provides a data line driving circuit ~~200 has~~that can include a shift resistor unit ~~210~~ in which respective shift resistor unit circuits Ua1 to Uan+2 are in cascade connection with each other. The circuit can also include~~, and~~ an output signal control unit ~~220 comprising~~having respective operational unit circuits Ub1 to Ubn+1. A NAND circuit ~~514~~ controls an enabling period of a negative sampling signal based on an output signal from a NAND circuit ~~511~~ in an subsequent-stage operational unit circuit.

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

---

(57) [Claim(s)]
[Claim 1] It has the liquid crystal panel by which the pixel electrode was connected to the data signal line through the switching element with which switching is controlled by the scanning signal line. It is the liquid crystal display of an active matrix with which the scanning signal-line drive circuit which impresses a scanning signal to two or more adjoining scanning signal lines simultaneously was prepared. About two adjoining scanning signal lines to which a scanning signal is impressed simultaneously Between the pixel electrodes of two trains connected to these scanning signal lines through the switching element, respectively A liquid crystal display equipped with the scanning signal timing-control circuit which terminates impression to timing earlier than the scanning signal which impressed the scanning signal impressed to the located scanning signal-line side to the scanning signal line of another side.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
(Field of the Invention)
this invention relates to the liquid crystal display of an active matrix used for the display of a color-television picture etc.
(Prior art)
By color-television methods, such as NTSC, the scan of one screen (frame) is divided into the odd number field and the even number field, and the interlace method which scans by jumping over the one scanning line at a time in each field is adopted. And in a liquid crystal display, when it is going to display such a video signal by the high resolution based on the interlace method, 2 simultaneous-scanning methods are used.
Here, the composition of the TFT active-matrix substrate in a liquid crystal display is shown in a view 7. This TFT active-matrix substrate connects the pixel electrode 12 to these in the shape of a matrix through TFT (TFT)15, respectively while forming many the scanning signal lines 13 and the data signal lines 14 on a substrate 11. Moreover, the common counterelectrode which is not illustrated is arranged through the liquid crystal layer at the opposed face of this TFT active-matrix substrate. The data signal of each data signal line 14 will be sent into the pixel electrode 12 connected to the scanning signal line 13 concerned by this composition through TFT15 through which it flowed when the scanning signal was impressed to each scanning signal line 13. And after impression of a scanning signal is completed and TFT15 intercepts, the potential of a data signal is held with the capacity of a liquid crystal layer etc. at each pixel electrode 12, and it comes to be updated by the degree this potential of whose is impression of a scanning signal. Therefore, even if it is the matrix method which impresses a scanning signal to a scanning signal line in order, in each pixel electrode 12, the potential of a data signal can always be held and it can be impressed by the liquid crystal layer.
It is made for the 2 above-mentioned simultaneous-scanning methods to impress a scanning signal to two adjoining scanning signal lines 13 simultaneously in such a liquid crystal display. Namely, as shown, for example in an octavus view , it sets to the scan of the odd number field. As a scanning signal is simultaneously impressed to the scanning signal line 13 of 1 Motome and 2 Motome first and a scanning signal is simultaneously impressed to the scanning signal line 13 of 3 Motome and 4 Motome later than a degree during the 1 horizontal scanning Make it impress a scanning signal to odd number Motome's scanning signal line 13, and the scanning signal line 13 of even number Motome located in this degree one by one simultaneously, and it sets to the scan of the even number field. A scanning signal is first impressed to 1 Motome's scanning signal line 13, and a scanning signal is simultaneously impressed to the scanning signal line 13 of 2 Motome and 3 Motome later than a degree during the 1 horizontal scanning. like the scanning signal line 13 of further 4 Motome and 5 Motome It is made to impress a scanning signal to two adjoining scanning signal lines 13 in which combination differs from the time of the scan of the odd number field simultaneously. Therefore, although the scanning signal line 13 and the pixel electrode 12 of **** are needed for the old scanning signal line 13 compared with the case of the simple scanning mode which impresses one scanning signal at a time, the picture of the high

resolution based on the interlace method can be acquired.
(Object of the Invention)
By the way, when a scanning signal is impressed to the above-mentioned scanning signal line 13, the potential of the pixel electrode 12 connected to this will fall rather than the potential of a data signal in response to the influence of the parasitic capacitance Cgd between the gate-drains in TFT15 at the time of the impression end of a scanning signal. That is, in the case of a simple scanning mode, when the gate voltage at the time of the flow in TFT15 and interception is set to VGHVGL, respectively and capacity of the liquid crystal layer in the pixel electrode 12 is set to CLC, only the potential deltaV about shown by the following formula (1) will fall rather than the potential of a data signal.
deltaV=(VGH-VGL) xCgd/(CLC+Cgd) -- (1)
But in the case of a simple scanning mode, such a potential fall is common about all the pixel electrodes 12. For this reason, if only fall potential deltaV shifts the opposite voltage impressed to a counterelectrode, it is easy to maintain to 0 DC balance of the voltage impressed to a liquid crystal layer by alternating current drive.
However, in the case of the 2 above-mentioned simultaneous-scanning methods, as shown in a view 9, you have to take into consideration the influence of the stray capacity Cpg between the scanning signal lines 13 which adjoin the side which is not connected to the pixel electrode 12 and this pixel electrode 12 besides a parasitic capacitance Cgd. That is, since change of potential also produces scanning signal-line 13b which adjoins the side which is not connected about such scanning signal-line 13a and pixel electrode 12a located among 13b with the scanning signal Sb when the scanning signals Sa and Sb are impressed to the scanning signal lines 13a and 13b of illustration, fall potential deltaV at the time of the impression end of the scanning signal Sa is shown by the following formula (2).
deltaV1= (VGH-VGL)
x(Cgd+Cpg)/(CLC+Cgd+Cpg) -- (2)
However, about pixel electrode 12b of another side, since the scanning signal is not impressed to scanning signal-line 13c which adjoins the side which is not connected yet and there is no change of potential, fall potential deltaV comes to be shown by the following formula (3).
deltaV2=(VGH-VGL) xCgd/(CLC+Cgd+Cpg) -- (3)
For this reason, in spite of connecting pixel electrode 12a and pixel electrode 12b to the same data signal line 14 and giving the same data signal voltage, the difference of delta V1 and delta V2 arises in the fall potential at the time of the impression end of a scanning signal, and, as for subsequent maintenance potential, the direction of pixel electrode 12b serves as high potential.
Therefore, in the conventional liquid crystal display, when a scanning signal was simultaneously impressed to two or more scanning signal lines, the difference arose in the luminosity of the pixel which adjoins on the same data signal line, and the problem that picture quality deteriorated had arisen.
this invention aims at offering the liquid crystal display which nonuniformity does not produce in the luminosity of a pixel in the drive method which impresses a scanning signal to two or more scanning signal lines simultaneously by shifting the impression end stage of the scanning signal in two scanning signal lines, and enabling it to hold potential on the conditions that each pixel electrode is the same, in view of the above-mentioned situation.
(The means for solving a technical problem)
The liquid crystal display of this invention is equipped with the liquid crystal panel by which the pixel electrode was connected to the data signal line through the switching element with which switching is controlled by the scanning signal line. It is the liquid crystal display of an active matrix with which the scanning signal-line drive circuit which impresses a scanning signal to two or more adjoining scanning signal lines simultaneously was prepared. About two adjoining scanning signal lines to which a scanning signal is impressed simultaneously It has the scanning signal timing-control circuit which terminates impression to timing earlier than the scanning signal which impressed the scanning signal impressed to the scanning signal-line side located between the pixel electrodes of two trains connected to these scanning signal lines through the switching element, respectively to the scanning signal line of another side. The above-mentioned purpose is attained by that.

(Operation)
When the scanning signals Sa and Sb are simultaneously impressed to the scanning signal lines 13a and 13b shown in a view 1 by the above-mentioned composition, the scanning signal Sb of pixel electrode 12a first connected to these scanning signal lines 13a and 13b and scanning signal-line 13b located among 12b ends impression previously in time t1. And since fall potential deltaV in pixel electrode 12b in this case does not have change of potential in scanning signal-line 13c like the conventional case, it is shown by the same following formula as the above-mentioned formula (3).
deltaV=(VGH-VGL) xCgd/(CLC+Cgd+Cpg) -- (4)
Moreover, after the scanning signal Sb of scanning signal-line 13b ends impression previously in this way, the potential of pixel electrode 12a which adjoins through stray capacity Cpg also once falls in response to influence. However, since TFT15 is still switch-on and pixel electrode 12a is connected to the data signal line 14 in this case, charge is performed immediately and it returns to the potential of a data signal again. And since the potential of scanning signal-line 13b which already adjoins has completed change after the scanning signal Sa of scanning signal-line 13a is late for the next time t2 and ending impression, it becomes the same conditions as the case of pixel electrode 12b, and fall potential deltaV also becomes the same value as the above-mentioned formula (4).
Consequently, since according to the liquid crystal display of this invention the potential fall at the time of the impression end of this scanning signal will become the same when a scanning signal is simultaneously impressed to two scanning signal lines, the potential which each pixel electrode holds becomes equal, and a uniform display image can be obtained.
In addition, in order to make uniform impression time of the scanning signal to each scanning signal line, you may make it also shift the timing of an impression start of a scanning signal according to the timing of this end. Moreover, when impressing a scanning signal to three or more scanning signal lines simultaneously, it can carry out similarly by shifting the timing of an impression end of a scanning signal in order between every two adjoining scanning signal lines.
(Example)
this invention is explained below about an example.
Views 2 are the timing diagram a view 2 or the 6th view shows one example of this invention, the block diagram of a liquid crystal display and a view 3 indicate the block diagram of a scanning signal-line drive circuit, and a view 4 indicates operation of a scanning signal-line drive circuit to be, the timing diagram which shows operation at the time of odd number field scanning [in / a liquid crystal display / in a view 5], and a timing diagram which shows operation at the time of even number field scanning / in / a liquid crystal display / in a view 6 In addition, ** which gives the same sign to the component which has the same function as the conventional example shown in the view 7 or the 9th view .
this example is a liquid crystal display for displaying the picture of color television of an NTSC color TV system on a liquid crystal panel.
The TFT active-matrix substrate of the liquid crystal panel 1 in a liquid crystal display forms much the pixel electrodes 12, the scanning signal lines 13, the data signal lines 14, and TFT15 on a substrate, as shown in the view 7 of the above. And each pixel electrode 12 is connected to the data signal line 14 which adjoins through between the source-drain terminals of TFT15 as shown in a view 1. Moreover, each of this TFT15 will flow through between source-drain terminals, if it connects with the scanning signal line 13 which a gate terminal adjoins and the scanning signal of high-level voltage is impressed to this scanning signal line 13.
Each scanning signal line 13 distributes even number Motome and odd number Motome of an every other to right and left, and the TFT active-matrix substrate of the above-mentioned liquid crystal panel 1 is pulled out, as shown in a view 2. And each scanning signal line 13 of this odd number Motome is connected to the scanning signal-line drive circuit 2, and each scanning signal line 13 of even number Motome is connected to the scanning signal-line drive circuit 3. These scanning signal-line drive circuits 2 and 3 consist of output buffers 2c and 3c which hold the output of the shift register circuits 2a and 3a to which a start signal is shifted one by one according to a clock signal, the level-shifter circuits 2b and 3b from which the output of these shift register circuits 2a and 3a is pulled up on level required for the

drive of TFT15, and these level-shifter circuits 2b and 3b, and are outputted to each scanning signal line 13, as shown in a view 3. Moreover, as shown in a view 2, the start signal which serves as the foundation of a scanning signal from the timing-control circuit 4, respectively, and the clock signal of a horizontal scanning period period are inputted into the shift register circuits 2a and 3a of these scanning signal-line drive circuits 2 and 3. Therefore, as shown in a view 4, the scanning signal to which the start signal was shifted one by one will be outputted to each scanning signal line 13 connected to these scanning signal-line drive circuits 2 and 3 [a horizontal scanning period every]. In addition, in this case, impression is started synchronizing with falling of a previous clock signal, and impression ends each scanning signal synchronizing with the standup of a next clock signal.

The above-mentioned timing-control circuit 4 outputs a start signal and a clock signal based on the synchronizing signal separated from the video signal. That is, about a start signal, synchronizing with a vertical synchronizing signal, at the time of the scan of the odd number field, it outputs to the scanning signal-line drive circuits 2 and 3 simultaneously, and only 1 horizontal scanning period delays and outputs the start signal to the scanning signal-line drive circuit 3 rather than the scanning signal-line drive circuit 2 at the time of the scan of the even number field. Moreover, a clock signal advances slightly the phase by the side of the scanning signal-line drive circuit 3 rather than the scanning signal-line drive circuit 2 at the time of the scan of the odd number field, at the time of the scan of the even number field, rather than the scanning signal-line drive circuit 2, delays slightly the phase by the side of the scanning signal-line drive circuit 3, and outputs it.

Operation of the liquid crystal display of the above-mentioned composition is based and explained in a view 5 and the 6th view .

When the scan of the odd number field is performed by the interlace method Since the start signal from the timing-control circuit 4 is simultaneously outputted to the scanning signal-line drive circuits 2 and 3 A scanning signal is first impressed to the scanning signal line 13 of 1 Motome and 2 Motome simultaneously. Next, only a horizontal scanning period will be overdue, a scanning signal will be simultaneously impressed to the scanning signal line 13 of 3 Motome and 4 Motome, and a sequential-scanning signal will be impressed to two scanning signal lines 13 of odd number Motome and even number Motome following this similarly hereafter. Moreover, when the scan of the even number field is performed, a start signal is previously outputted to the scanning signal-line drive circuit 2 from the timing-control circuit 4, only 1 horizontal scanning period is late for the scanning signal-line drive circuit 3, and a start signal is outputted. For this reason, when a scanning signal is first impressed to 1 Motome's scanning signal line 13, later than a degree only in a horizontal scanning period, a scanning signal will be simultaneously impressed to the scanning signal line 13 of 2 Motome and 3 Motome, and a sequential-scanning signal will be henceforth impressed to two scanning signal lines 13 of even number Motome and odd number Motome following this. Consequently, the display of the scanning line of odd number Motome and even number Motome following this is performed in the odd number field, the display of the scanning line of even number Motome and odd number Motome following this will be performed, and each pixel of a liquid crystal panel 1 can display now the picture of the high resolution by 2 simultaneous-scanning methods which applied to the interlace method correspondingly by this in the even number field.

Moreover, in the above-mentioned odd number field, in order that the timing-control circuit 4 may advance slightly the phase of the clock signal to the scanning signal-line drive circuit 3, as for the scanning signal impressed simultaneously, even number Motome's scanning signal line 13 starts impression early slightly rather than odd number Motome's scanning signal line 13 in fact, and an impression end stage also becomes early. Therefore, in the scan of this odd number field, scanning signal-line 13a shown in the view 1 will correspond to odd number Motome's scanning signal line 13, and scanning signal-line 13b will correspond [even number Motome] scanning signal-line 13. For this reason, since the potential of the scanning signal line 13 (13c) which the potential held at the pixel electrode 12 (12b) connected to even number Motome's scanning signal line 13 (13b) which impression of a scanning signal ends previously adjoins and which is not connected does not change, only the fall potential deltaV shown by the aforementioned formula (4) becomes a low value from the potential of a

data signal. And in order that the scanning signal line 13 (13b) of the point which the potential held at the pixel electrode 12 (12a) connected to odd number Motome's scanning signal line 13 (13a) which impression of a scanning signal ends later than this also adjoins and which is not connected may already have finished changing potential, only the same fall potential deltaV as the above becomes a low value. Furthermore, in the above-mentioned even number field, in order that the timing-control circuit 4 may delay slightly the phase of the clock signal to the scanning signal-line drive circuit 3, as for the scanning signal impressed simultaneously, odd number Motome's scanning signal line 13 starts impression early slightly rather than even number Motome's scanning signal line 13 in fact, and an impression end stage also becomes early. Therefore, in the scan of this even number field, scanning signal-line 13a shown in the view 1 will correspond to even number Motome's scanning signal line 13, and scanning signal-line 13b will correspond to odd number Motome's scanning signal line 13. For this reason, since the potential of the scanning signal line 13 (13c) which the potential held at the pixel electrode 12 (12b) connected to odd number Motome's scanning signal line 13 (13b) which impression of a scanning signal ends previously adjoins and which is not connected does not change, only the fall potential deltaV more nearly same than the potential of a data signal as the above becomes a low value. And in order that the scanning signal line 13 (13b) of the point which the potential held at the pixel electrode 12 (12a) connected to even number Motome's scanning signal line 13 (13a) which impression of a scanning signal ends later than this also adjoins and which is not connected may already have finished changing potential, only the same fall potential deltaV as the above becomes a low value.
Since the conditions at the time of the impression end of this scanning signal become the same for every scanning line and the potential which each pixel electrode 12 holds becomes equal when a scanning signal is simultaneously impressed to two scanning signal lines 13 with 2 simultaneous-scanning methods according to the interlace method according to the liquid crystal display of this example the above result, the uniform display screen can be obtained.
(Effect of the invention)
Since the potential fall at the time of the impression end of these scanning signals can be made the same when a scanning signal is simultaneously impressed to two or more adjoining scanning signal lines according to the liquid crystal display of this invention so that clearly from the above explanation, the potential which each pixel electrode holds becomes equal, and a uniform display image can be obtained.

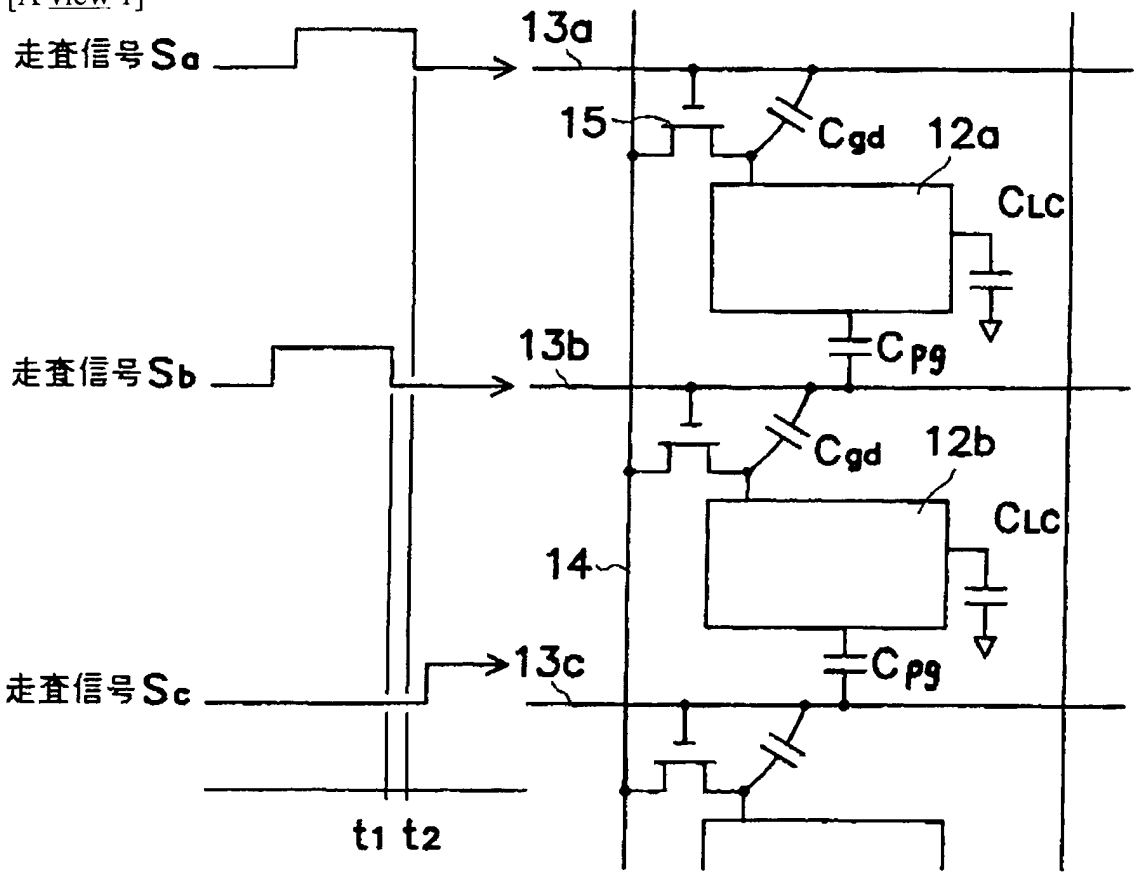
[Translation done.]

* NOTICES *

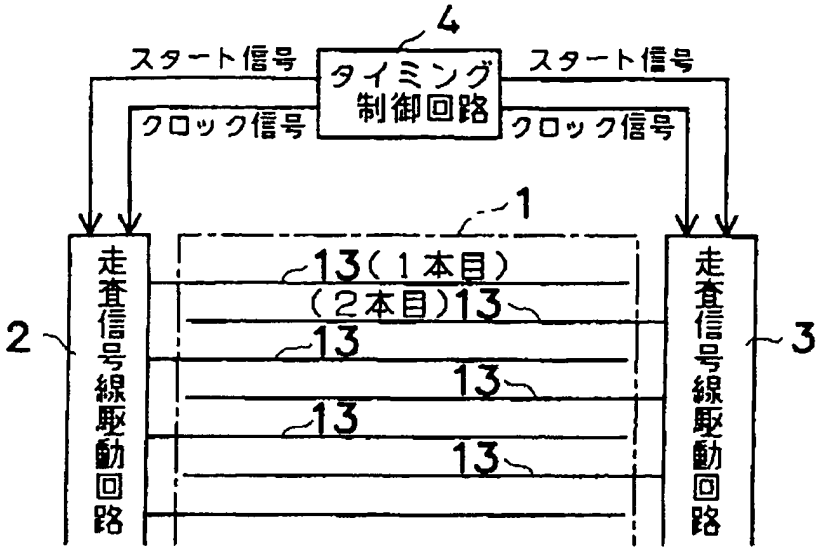
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

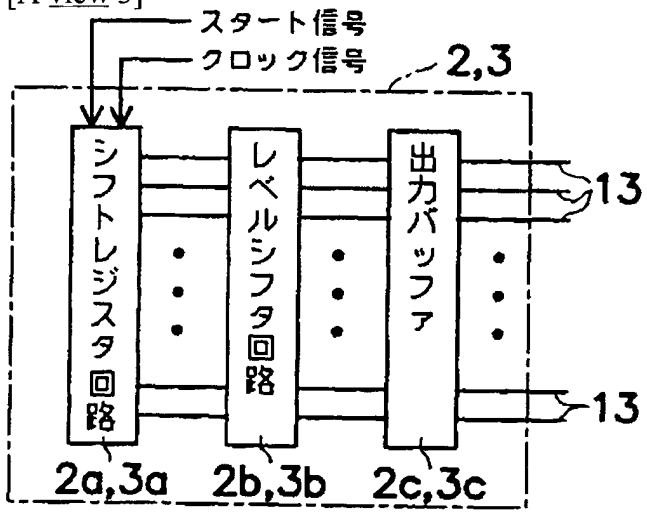
[A view 1]



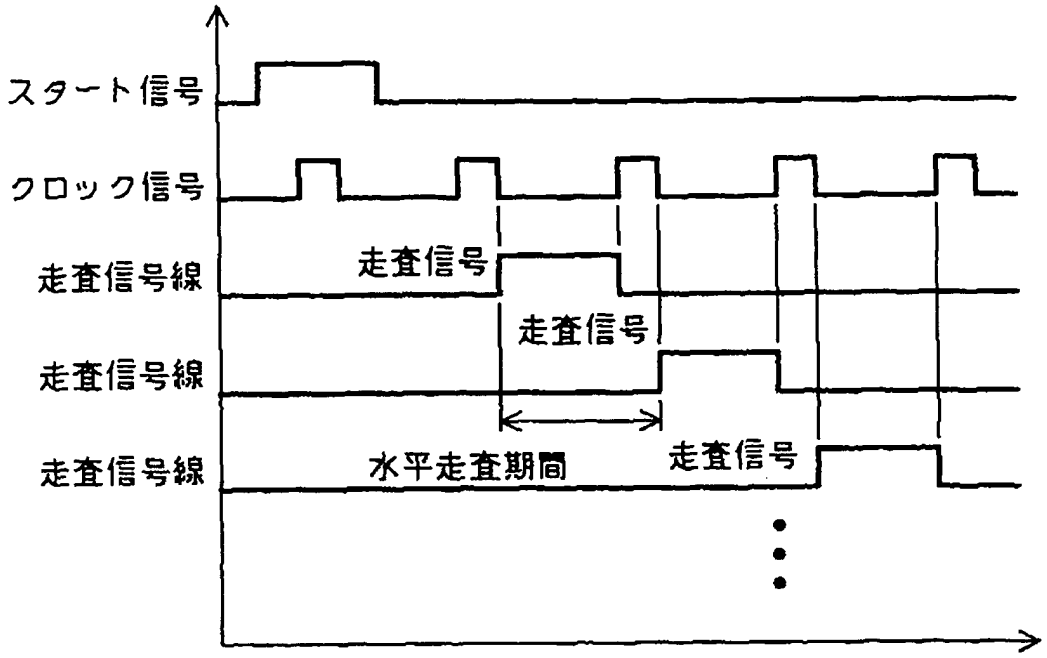
[A view 2]



[A view 3]

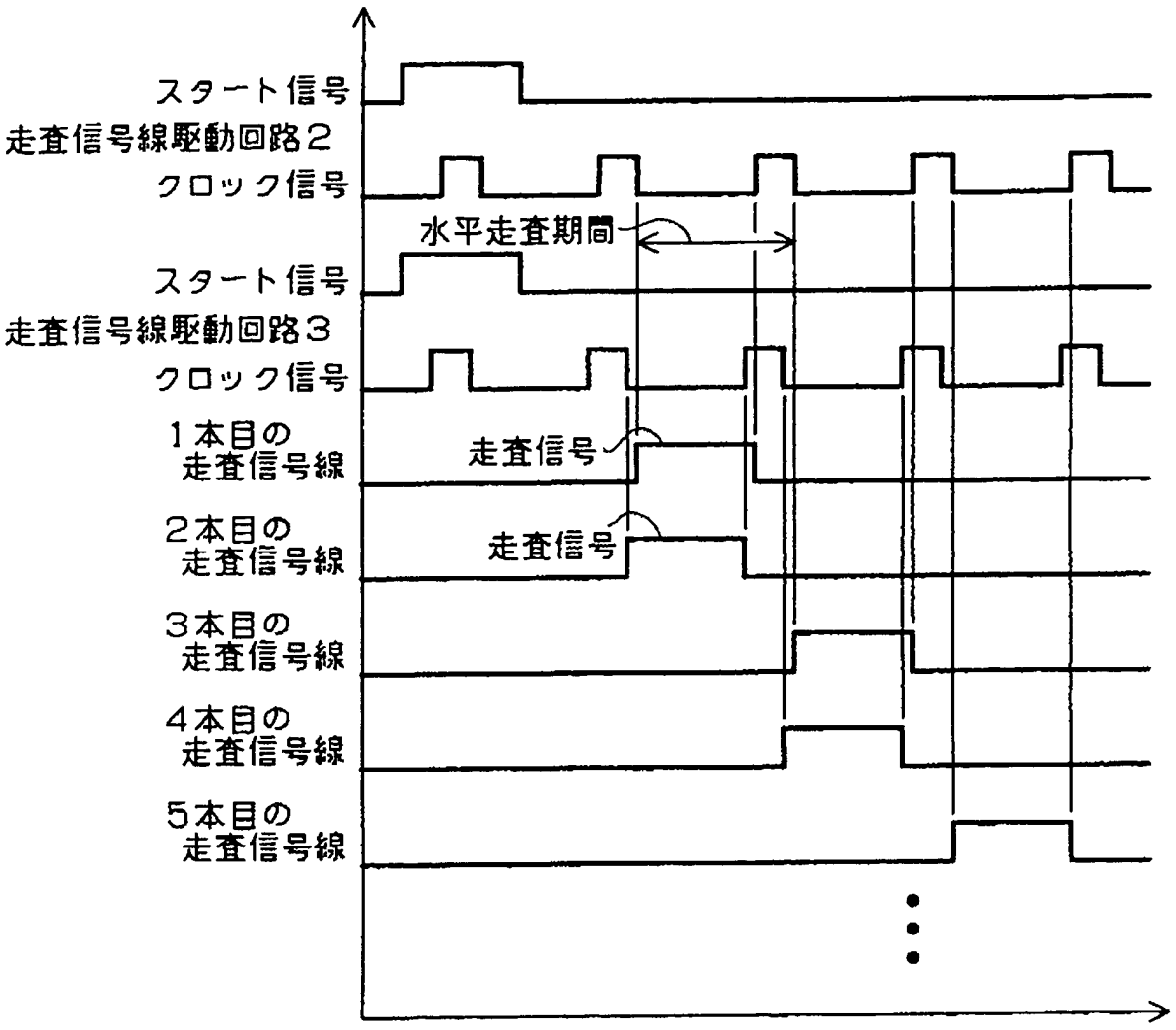


[A view 4]



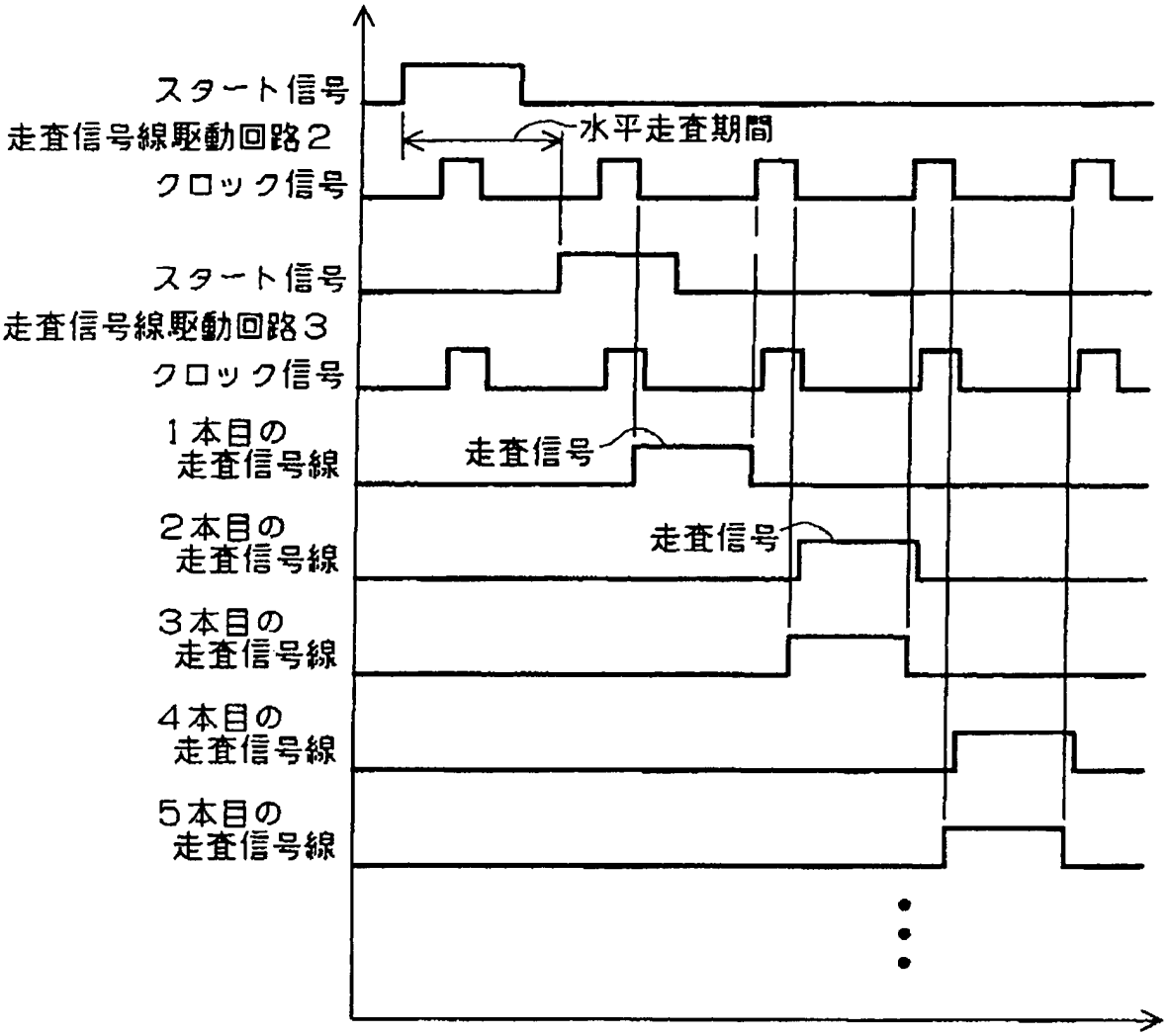
[A view 5]

奇数フィールド走査時

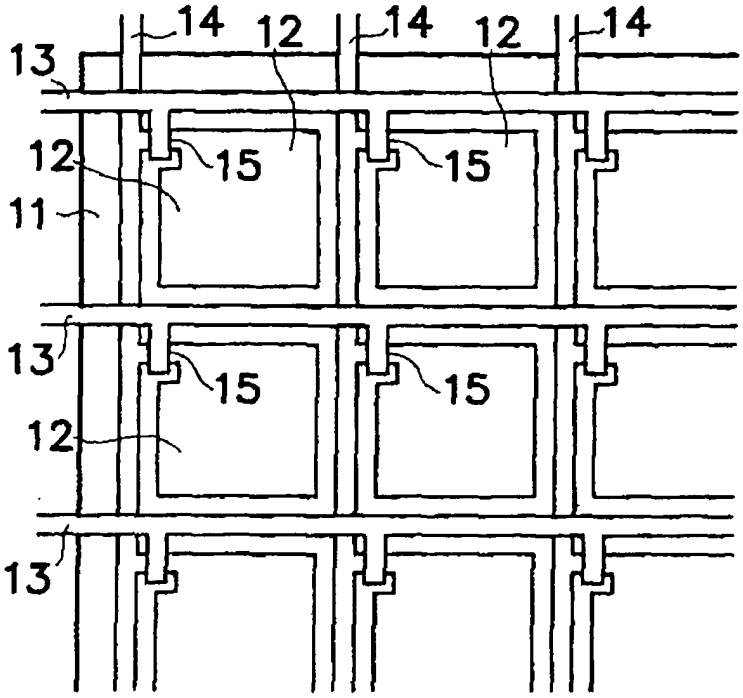


[A view 6]

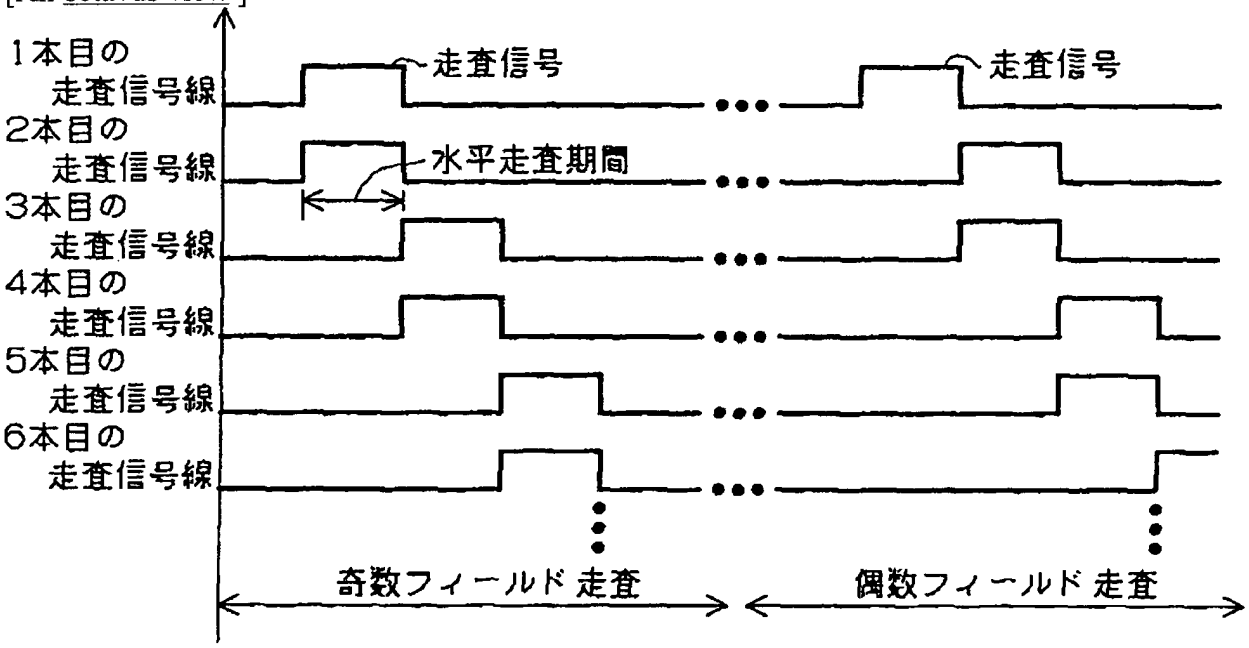
偶数フィールド走査時



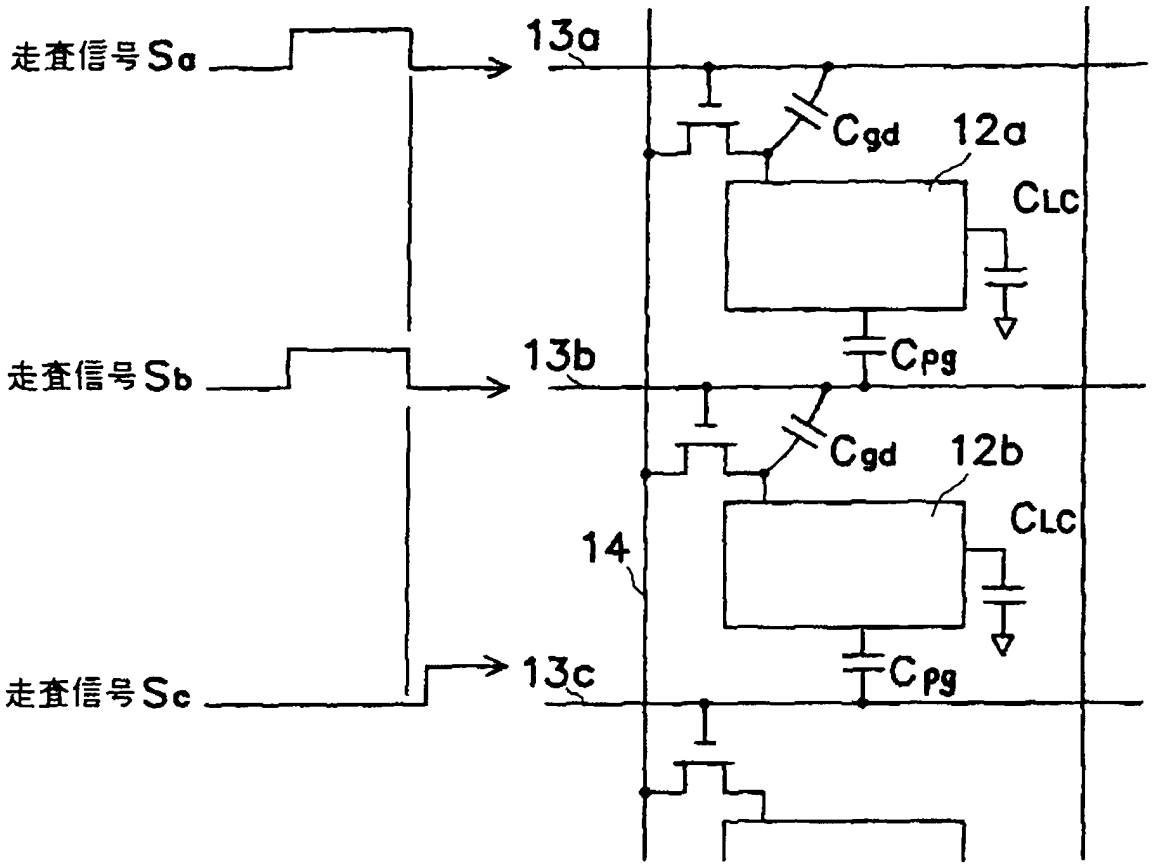
[A view 7]



[An octavus view]



[A view 9]



[Translation done.]